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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,070	02/03/2006	Michiel Jos Van Duuren	NL03 0977 US1	9477

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EXAMINER	
LAPPAS, JASON	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
10/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/567,070	VAN DUUREN, MICHIEL JOS	
	Examiner	Art Unit	
	JASON LAPPAS	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *** has been entered.

Response to Amendment

Applicant's amendment dated 10/02/2008 in which claims 5, 8, and 11-13 were amended and claims 16-21 were added has been entered of record. Currently, claims 1-21 are pending in light of the amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 6, and 14-16 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Krishnamurthy (U.S. Patent 6,233,178).

Claim 1. Method for operating an array of nonvolatile charge
trapping memory devices (Memory Array of Flash Cells Krishnamurthy Fig 1), comprising:
before block erasing the array by discharging substantially all of the non-volatile charge trapping memory devices of the array (In process 300 Krishnamurthy Fig 3 Precondition 310 is taught before erase 320. Pre-condition discharges cells as taught in Col 4 lines 43-45. Process 300 of figure is for each sector, or block, 110 or memory 100 fig 1), block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array (330 Programming Fig 3 300 of figure is for each sector, or block, 110 or memory 100 Krishnamurthy fig 1).

Claim 2. Method according to claim 1, furthermore comprising after the erase operation programming some of the non-volatile memory devices of the array depending on data content to be stored in the non-volatile memory devices of the array (330 Programming after erase 320 Krishnamurthy Fig 3).

Claim 5. An electrical device comprising
an array of non-volatile charge trapping memory devices (Memory Array of Flash Cells Krishnamurthy Fig 1), and a memory control (Control Circuit of Krishnamurthy Fig 5)

arranged to control block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array (330 Programming Fig 3 300 of figure is for each sector, or block, 110 or memory 100 Krishnamurthy fig 1, memory also taught in Krishnamurthy Fig 5), control block erasing the array by discharging substantially all of the programmed non-volatile charge trapping memory devices of the array (Erase 320 is taught in process 300 Krishnamurthy Fig 3. Process 300 of figure is for each sector, or block, 110 or memory 100 Krishnamurthy fig 1), and
control the array of non-volatile charge trapping memory devices such that before block erasing of substantially all of the non-volatile memory devices of the array, substantially all of the non-volatile memory devices of the array are block programmed (In process 300 Krishnamurthy Fig 3 Precondition 310 is taught before erase 320. Pre-condition includes a short write, writing is programming, cells as taught in Col 4 lines 43-45. Process 300 of figure is for each sector, or block, 110 or memory 100 Krishnamurthy Fig 1).

Claim 6. An electrical device according to claim 5, wherein the non-volatile memory device comprises a transistor having a channel and a control gate, a dielectric charge trapping layer being located between the channel and the control gate (Krishnamurthy Fig. 2).

Claim 14. An electrical device according to claim 5, wherein the array of non-volatile memory devices forms a non-volatile memory (as seen in Krishnamurthy Fig 5).

Claim 15. A method according to claim 1, wherein the non-volatile memory devices of the array each include a dielectric charge trapping layer and wherein block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array includes trapping charge in the dielectric charge trapping layers (Charge trapping layers taught in ONO cell Fig 2. Process 300 of figure is for each sector, or block, 110 or memory 100 Krishnamurthy Fig 1).

Claim 16. A method for use with programming an array of non-volatile charge trapping memory devices (Memory Array of Flash Cells Krishnamurthy Fig 1) according to data content to be stored therein, the method comprising, prior to substantially every programming step (330 Programming Krishnamurthy Fig 3):

block programming substantially all of the non-volatile charge trapping memory devices of the array (In process 300 Krishnamurthy Fig 3 Precondition 310 is taught before erase 320. Pre-condition includes a short write, writing is programming, cells as taught in Col 4 lines 43-45. Process 300 of figure is for each sector, or block, 110 or memory 100 Krishnamurthy fig 1); and

after the block programming step, block erasing substantially all of the non-volatile charge trapping memory devices of the array (Erase 320 before Programming 330 Krishnamurthy Fig 3).

Claim 21. The method of claim 1, wherein the array is operated such that substantially none of the non-volatile charge trapping memory devices experiences two consecutive discharging cycles without experiencing an intermediate charging cycle (before every erase 230 Fig 3 there is a precondition 310 therefore substantially none of the non-volatile charge trapping memory devices experiences two consecutive discharging, or erase, cycles).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7-9, 11, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy (U.S. Patent 6,233,178) in view of Guliani (U.S. Patent 6,366,497).

Claim 3. Krishnamurthy discloses method of claim 2 and 16 and device of claim 5 but does not disclose reference cells.

Guliani discloses reading the data content stored in a non-volatile memory device of the array, wherein for reading the data content stored in a non-volatile memory device of the array at least one further non-volatile memory device having a dielectric charge trapping layer (Flash cell 270 taught in Guliani Fig 1) is used as reference cell which is programmed and erased for a block programming and block erase, respectively, of the non-volatile memory devices in the array (Guliani Col 4 lines 18-26 teaches the reference cell is programmed for both programming and erasing configurations) for the purpose of supplying reference voltage to the sense amplifier (Guliani Col 4 lines 18-26).

Since Krishnamurthy and Guliani are both from the same field of endeavor (Flash memory), the purpose disclosed by Guliani would have been recognized in the pertinent art of Krishnamurthy.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the reference circuit taught by Guliani in the circuit taught by Krishnamurthy for the purposes of supplying reference voltage to the sense amplifier (Guliani Col 4 lines 18-26).

Claim 7. An electrical device according to claim 5, the array being provided with at least one non-volatile memory device for use as a reference cell in a sense amplifier (Flash

cell 270 taught in Guliani Fig 1, same motivation to combine as claim 3).

Claim 8. An electrical device according to claim 7, the array comprising circuitry arranged to program and erase the reference cell for a block-programming and block-erasing respectively of the non-volatile memory devices in the array (Guliani Col 4 lines 18-26 teaches the reference cell is programmed for both programming and erasing configurations).

Claim 9. An electrical device according to claim 7, wherein the at least one reference cell is separate from the array (Separate flash cell 270 taught in Guliani Fig 1, same motivation to combine as claim 3).

Claim 11. An electrical device according to claim 7, comprising means circuitry arranged to compare (Sense amp 160 Guliani Fig 1) a read current from a non-volatile memory device (110 Guliani Fig 1) in the array with a read current from the reference cell (150 Guliani Fig 1).

Claim 17. The method of claim 16, further comprising programming a reference memory cell each time the block programming step is performed (Guliani Col 4 lines 18-26 teaches the reference cell is programmed for programming configurations. Process 300 of figure is for each sector, or block, 110 or memory 100 Krishnamurthy fig 1), and erasing the reference memory cell each time the block erasing step is performed

(Guliani Col 4 lines 18-26 teaches the reference cell is erased for erasing configurations), wherein the reference memory cell is a non-volatile charge trapping memory device (same motivation to combine as claim 3).

Claim 20. The method of claim 17, wherein the reference memory cell has a programming and erasing history that matches the block programming and blocking erasing history of the array (this is inherent since the reference cell and the blocks are programmed and erased at the same time).

Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy (U.S. Patent 6,233,178) in view of Guliani (U.S. Patent 6,366,497) further in view of Takahashi (U.S. Patent 6,639,849).

Claim 4 and 10. Krishnamurthy and Guliani teach method of claim 3 and device of claim 7 but do not disclose wherein the memory devices of the array together function as reference cells.

Takahashi discloses memory devices of the array together function as reference cells (Takahashi Fig 2) for the purpose of judging a level of read data (Takahashi, Abstract).

Since Krishnamurthy, Guliani and Takahashi are from the same field of endeavor (Flash memory), the purpose disclosed by Takahashi would have been recognized in the pertinent art of Krishnamurthy and Guliani.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use memory devices of the array together function as reference cells as taught by Takahashi in the circuit taught by Krishnamurthy and Guliani for the purposes of judging a level of read data (Takahashi, Abstract).

Claims 12,13, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy (U.S. Patent 6,233,178) in view of Guliani (U.S. Patent 6,366,497) further in view of Kurihara (U.S. Patent 6,791,880).

Claim 12. Krishnamurthy and method of claim 16 and Krishnamurthy and Guliani disclose the device of claim 7 but they do not disclose circuitry arranged to adapt a read current for reading the non-volatile memory devices in the array to the ageing of the reference cell.

Kurihara discloses circuitry arranged to adapt a read current for reading the non-volatile memory devices in the array to the ageing of the reference cell (Kurihara Col 2 lines 32-35) for the purpose of providing current after aging (Kurihara Col 2 lines 39-40).

Since Krishnamurthy, Guliani and Kurihara are from the same field of endeavor (Flash memory), the purpose disclosed by Kurihara would have been recognized in the pertinent art of Krishnamurthy and Guliani.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the life simulation circuit taught by Kurihara in the circuit

taught by Krishnamurthy for the purposes of providing current after aging (Kurihara Col 2 lines 39-40).

Claim 13. An electrical device according to claim 7, comprising circuitry arranged to adapt a required control gate voltage for reading the non-volatile memory devices (Kurihara teaches adapting current source Col 2 lines 32-35. Current and gate voltage are directly related as addressed in Col 2 lines 15-21) in the array depending on the ageing of the reference cell (Kurihara Col 2 lines 39-40).

Claim 18. The method of claim 17, further comprising comparing a read current from a selected non-volatile memory device in the array with a read current from the reference memory cell (comparison of read current from memory and reference cell taught in Kurihara Col 2 lines 32-35).

Claim 19. The method of claim 18, further comprising adapting the read current from the selected non-volatile memory device based on the read current from the reference memory cell (adapting the read current from memory and reference cell taught in Kurihara Col 2 lines 35-40).

Response to Arguments

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Lappas whose telephone number is (571)270-1272. The examiner can normally be reached on M-F 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. L./
Examiner, Art Unit 2827
/AMIR ZARABIAN/
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